Opportunities for the Printing Industry in Electronics: The Low Cost Semiconductor Fab of the Year 2012

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Abstract: Many organic field effect transistor (OFET) printing processes developed in the laboratory environment are not easily transferable to high-volume manufacturing. Studies are underway to assess the ability to manufacture organic electronics using off-the-shelf contact and non-contact printing platforms to fabricate OFETs using solution-processable organic semiconductor materials and traditional materials presently available and qualified for use in microelectronic products.

Introduction

The recent enhancements of organic semiconductor material stability and processability [1-3] have resulted in the fabrication of high-performance organic electronics in laboratory environments. Several organic semiconductor materials are presented in Fig 1. These materials have demonstrated improved processing properties as well as performance when exposed to ambient conditions. In general, organic semiconductor materials have similar development maturity trends that can be divided into three distinct periods (Fig. 2). The first period is labeled "discovery" and designates the introduction of a new class or family of organic materials. This stage is followed by a "process

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management" period during which engineers and scientists develop methods and procedures to process organic semiconductor films that yield OFETs demonstrating improved performance. The final stage is referred to as "saturation" beyond which device performance is only incrementally improved. It is generally agreed upon that "saturation" is achieved when device performance is bounded by intrinsic material electrical properties.

Since their proof of concept in 1986, the OFET and related technologies have progressed in recent years to a point where they are becoming attractive for practical industrial applications. Most notably, increases in carrier mobility, environmental stability, and advancements in p- and n-type materials have resulted in reports of device operation suitable for low-functionality, low-cost products. The technology has become even more attractive after the demonstration of solution-processable materials. These open the door to low-cost deposition techniques such as screen printing, spin coating, and conventional graphics arts printing technologies.

The improved device performance was essential for potential applications to be realized, *i.e.*, RFID transponder circuits and display driver circuits [4-7]. The market opportunities for many of these applications depend on cost (direct materials and conversion). To achieve these cost targets, the low-cost materials and processes developed in the laboratory have to be transferable to the high-volume manufacturing environment. A proposed high-volume manufacturing platform is based on the integration of commercially available printing technologies to fabricate organic circuits directly on low-cost substrates in reel-to-reel formats. These manufacturing methods and the use of a continuous flexible material are key solutions for manufacturing low-cost OFET based products. The cost of building a new silicon semiconductor fabrication facility has steadily risen and now approaches $3B [8]. The high cost is partially due to the "clean-room" environment, costly aggressive chemical distribution facilities and plumbing, wafer processing and handling equipment, and wafer testing equipment. For example, a wafer processing vacuum chamber and a processed silicon wafer is presented in Fig. 3. More recently, as organic semiconductor materials have demonstrated reliability and enhanced performance, engineers have suggested that an organic semiconductor fabrication facility could be built for $40MM [8]. Unlike silicon fabrication facilities, an organic semiconductor facility would use traditional graphics arts printing platforms to deposit the materials in a non-

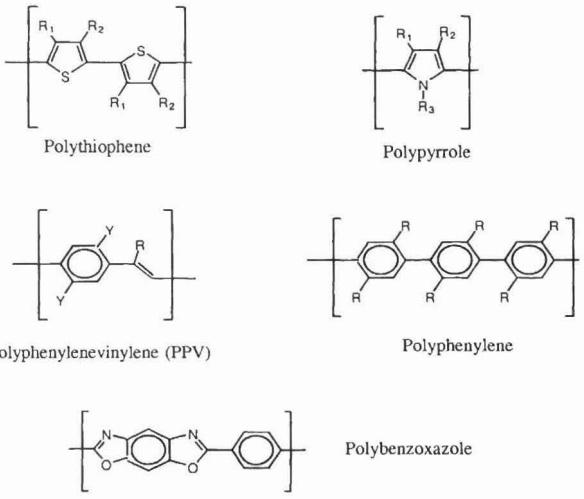


Figure 1. Chemical structures for organic semiconductor materials.

cleanroom manufacturing facility. An OFET processing platform and a processed OFET device is presented in Fig. 4.

This effort is evaluating several low-cost, high-volume electronics manufacturing and graphic arts printing technologies, and their utilization for the deposition of commercially available material systems for fabricating OFETs. The printing technologies evaluated represent two general categories:

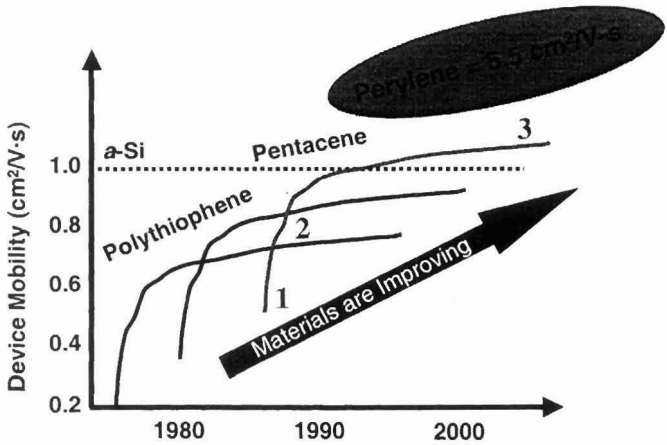


Figure 2. Organic semiconductor development maturity trend: 1) Discovery, 2) Process management, and 3) Saturation.

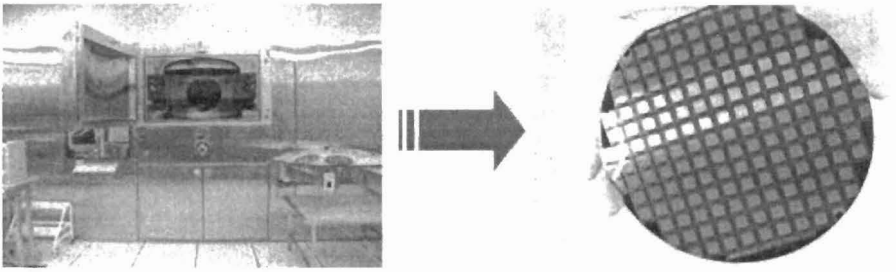


Figure 3. Traditional silicon wafer fabrication. Left – Example silicon wafer processing platform. Right – Fabricated 4inch electrically functional silicon wafer.

non-contact printing (ink jet printing, micro-dispensing, and spin coating), and contact printing (pad printing, flexographic printing, and screen printing). The

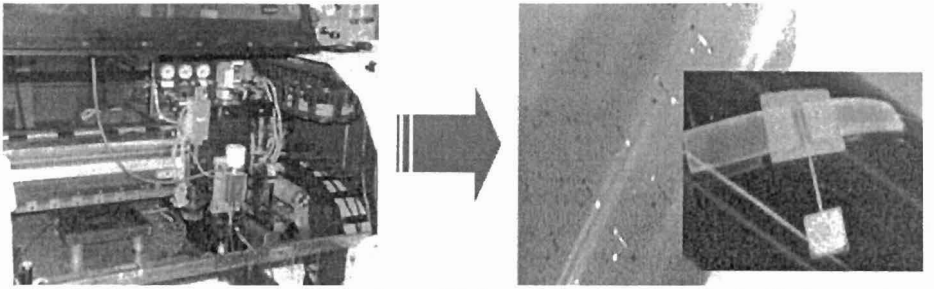


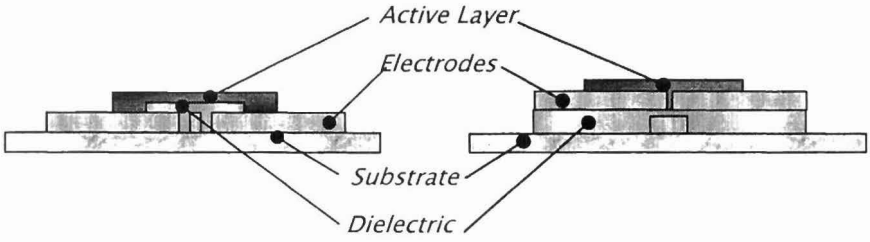
Figure 4. Proposed organic transistor fabrication. Left – Example high speed ink jet printing platform. Right – A printed OFET on a flexible substrate.

following material systems were studied during the fabrication of OFET structures: polymer thick film (PTF), nano-particle dispersions, conductive polymers and organo-metallics as electrodes; PTF dielectrics and dielectric polymers as dielectrics; solution-processable organic semiconductors as the active layer; and polyimide and polyester as the substrates.

OFET Device Structures

The OFET structures that were used are based on thin film transistor architectures and are illustrated in Fig. 5. The three-layer construction (Structure 1, Fig. 5a) requires three printing steps while the four-layer construction

(Structure 2, Fig. 5b) requires four printing steps. Clearly, the advantages of printing Structure 1 were fewer printing steps, reduced process compatibility issues and fewer opportunities for layer-to-layer interface incompatibility. However, Structure 1 can only be electrically operated in depletion mode while structure 2 can be operated in both depletion and accumulation modes (depending on the semiconduting polymer properties).



(a) Structure 1 (b) Structure 2

Figure 5. Transistor Structures

Manufacturing Technologies

OFET devices are comprised of conductive, dielectric, and active materials layers. A low cost fabrication method is the use of direct material deposition technologies. These technologies were categorized as 1) contact and 2) non-contact printing. An example contact printing system is shown in Fig. 6 while an example non-contact printing system is shown in Fig. 7. Both figures also show OFET device structures that were fabricated using commercially available printing systems and materials. The contact printing system was used to fabricate the electrodes of the OFET (source, gate, and drain) using a high viscosity polymer thick film filled with conductive material (Fig. 6). Figure 7 shows a gate electrode and contact pad that was fabricated with the non-contact system and a nanoparticle suspension. A materials/printing platform matrix is presented that classifies the different printing processes, materials systems, and feature size limitations (Table 1).

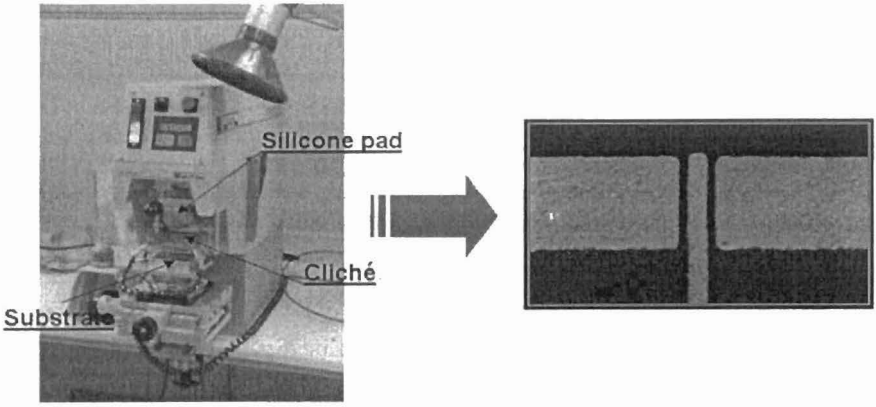


Figure 6. Contact printing platform. Right – Example of a system for high viscosity materials. Left – Fabricated OFET structure elements (source, gate, drain).

Realizing the diversity of the materials (conductor, insulator, and semiconducting polymer) required to fabricate functional transistors, a combination of contact and non-contact printing technologies was used during OFET fabrication. The selection of printing technologies was

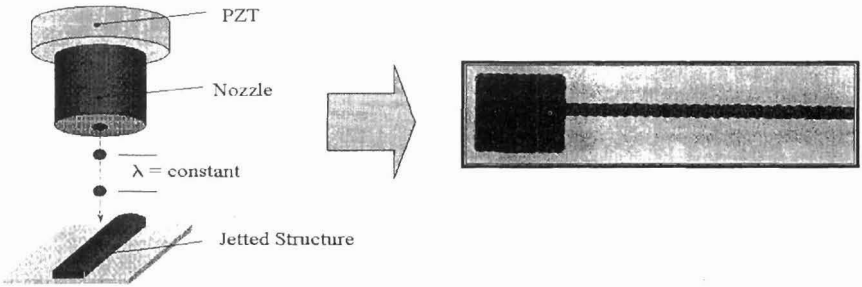


Figure 7. Non-contact printing platform. Right – Example of a system for low viscosity materials. Left – Fabricated OFET structure elements (gate and contact pad).

based on the material rheological properties, commercial availability of the materials, material thermal curing schedule, and solvent compatibility for the sequential printing operations.

Some of the commercially available materials used for the different printing technologies are listed in Table 1. Polymer thick film (PTF) conductors and dielectrics were epoxy resins filled with metal or dielectric particles. The PTF

pastes were deposited using stencil, pad printing, flexographic, and/or micro-dispensing printing. The low viscosity polymer solutions and nanoparticle suspensions were printed by ink jetting and/or spin coating. Material rheological properties determined the selection of printing technology used: the pastes with high viscosity and large-sized particles were deposited by contact printing, yielding thick film structures. Lower viscosity solutions and nanoparticle suspensions were non-contact printed and yielded thin film structures.

Table 1. Manufacturing processes and materials systems.

Process	***Materials***	***Feature Size***	***Printing Type***
Flexographic	PTF conductor and dielectric	50 μm Line/Space	Contact Printing
Stamping			
Stenciling		100 μm Line/Space	
Dispensing			Non-Contact Printing
Jetting	Nano particle inks; Conductive and dielectric polymers; Organic semiconductors	75 μm Line/Space	
Spin Coating	Organic semiconductors		

Printed OFET Devices

Organic transistor performance for a given semiconducting polymer can vary by a few orders of magnitude depending on device fabrication processes and materials (conductor, semiconductor, and dielectric). The manufacturing challenges in fabricating sequentially built-up structures were: 1) to ensure process compatibility between processes, and 2) to ensure material compatibility between layers. In particular, materials with low curing temperatures are required not only for achieving low cost but also for eliminating material degradation when subjected to the multiple curing processing steps. In addition, the deposited films must be insensitive to composition (*e.g.*, solvents) of the subsequently deposited materials in order to maintain adequate electrical and mechanical properties. A few candidate materials (conductors, dielectrics, and organic semiconductors) were studied and OFETs using a combination of materials systems were successfully fabricated. An example of a printed OFET using commercial materials and printing platforms is shown in Fig. 8. Similar structures have shown reproducible electrical performance with mobility ranging from 10^{-5} to 10^{-3} cm^2/Vs depending on the printing technology, and the materials used.

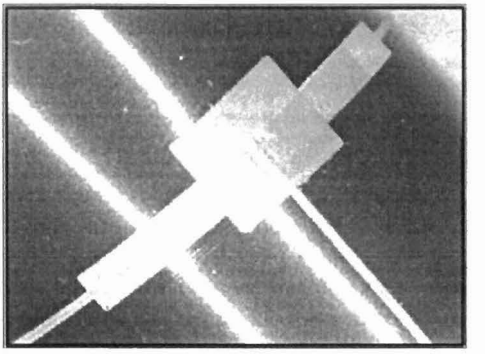


Figure 8. An All Printed OFET (Structure 1)

Device Testing Strategies

Standard testing methodology must support the needs of electronics product designers in addition to the research scientist. While in the past device performance was quoted in terms of device mobility and on-off ratio, these values give minimal information to electronics circuit designers. Additional parameters beneficial to designers (e.g., gain, leakage, parasitic capacitances, etc.) need to be evaluated. Frequency-dependent behavior for organic devices also must be more extensively measured, as this directly affects circuit design and provides greater meaning to a designer rather than carrier mobility values.

Another needed area for development is for in-line electrical testing that is critical for deposition and quality control. These tests are required for evaluating the variation in the deposition process, assisting in readjustment of process controls and maximizing yield, which directly affects final product unit cost. Standardization of testing on the manufacturing floor would allow standard operating procedures (SOPs) to be developed for various scenarios. This minimizes the guesswork and knowledge required by personnel operating the deposition equipment. The development and implementation of automatic feedback controls would further reduce the demands placed on the operator, which will increase product quality and yield.

Successful implementation of organic electronic technology requires that data to product groups adhere to industry-standard design practices. These include device models that are compatible with standard circuit design software packages, such as SPICE. Such models require knowledge of expected value tolerances and their variation with temperature. These models are critical to the acceptance of organic electronic technology by the design engineering

establishment. Development of n-type materials that are compatible with current p-type technology is also critical for the adoption of organic electronic technology: this maximizes leveraging of existing circuit designs and brings organic electronic design on par with established circuit design practices.

Reliability performance needs to be reported to electronic product groups so that expected product lifetimes may be predicted. Reliability performance data for organic transistors may follow industry-standard reporting methods (i.e., Electronic Industries Association Joint Electron Device Engineering Council – EIA/JEDEC), or may require different standards due to the unique properties of organic materials. For example, organic electronics have been found to be particularly sensitive to light, oxygen, moisture, and other environmental conditions. A standard method of evaluating these effects on electrical performance and then reporting this information must be set.

The development and implementation of electrical design and testing methodologies that are compatible with manufacturing: standardized design rules and methods; material, device, and design tolerances/variations; and testability of products during and after manufacture is critical for the acceptance and diffusion of OFET technology into the mainstream.

OFET Technology Diffusion

In general, the advances in OFET technology were primarily conducted in a controlled research laboratory environment. Moreover, attainable device performance found in the literature is generally best-case and sometimes difficult to repeat reliably since reported device performance for a given material and process can vary by many orders of magnitude. The testing methodology practiced to obtain this information is largely non-standardized, which may at best complicate the comparison of device performance between different organizations, or even render such comparisons meaningless. Therefore, objective comparisons of deposition techniques may be problematic. Acceptable transistor performance often requires a high level of control and care during deposition. While this is perfectly acceptable for proof-of-concept and in research environments, it is not transferable to the manufacturing floor (Fig. 9). In a manufacturing environment, the available levels of control and cleanliness are typically lower.

This difference is particularly apparent when various processing techniques are evaluated. One important attribute for evaluating deposition techniques is feature size. Reduced feature size is critical for improved device performance: this is particularly apparent in the silicon world where carrier mobility has not significantly changed over many years but reduced feature size

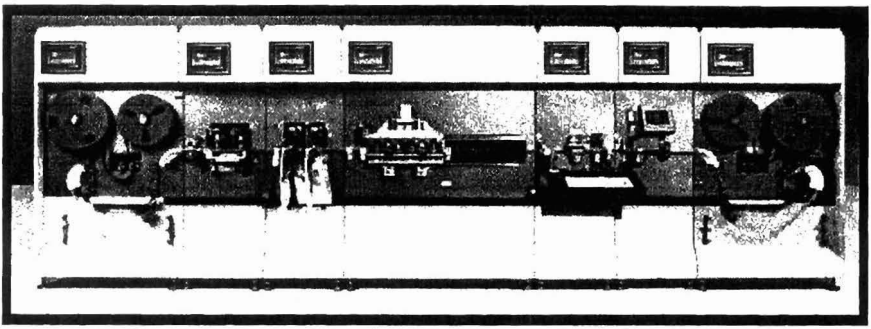


Figure 9. Proposed modular OFET web-based manufacturing platform.

has resulted in very significant performance improvements. Conventional, manufacturing-compatible printing techniques are typically limited to 50-100 μm. Though novel printing techniques such as micro-contact printing demonstrate feature sizes approaching 1 μm, making the techniques compatible with standard manufacturing practices has so far not been demonstrated.

In order to transfer organic electronic technology from the laboratory to the manufacturing floor, many design, testing, and reliability issues need to be addressed. Standardized testing methodology and device specification methods need to be established so that meaningful comparisons can be made between different organizations and deposition practices. The installation of such standards may best be accomplished through one or more established standards organizations (e.g., Institute of Electrical and Electronics Engineers - IEEE, Technical Association of the Graphics Arts - TAGA, The American Society for Testing and Materials - ASTM, etc.). Rules for design for testability and quality-monitoring controls are needed through such standards.

Conclusions

Several contact and non-contact printing platforms in combination with various commercially available materials were used to fabricate electrically active OFETs. The electrical performance of these OFET devices were strongly dependent on several materials and processing parameters. Several efforts are underway to identify the optimal materials and processing parameters to create preferred technology suites. In addition, several printing service suppliers and equipment providers are being contacted to investigate opportunities for transferring the technology from an R&D environment to pilot/manufacturing environment.

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